AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions of claims in the application.

Claim 1 (Currently amended): A method of manufacturing a semiconductor device, comprising the steps in the following order [[of]]:

(a) preparing a semiconductor substrate having current input/output regions;

(b) forming an insulating layer on the semiconductor substrate, ~~said insulating layer covering said current input/output regions;~~

(c) forming a resist laminate on the insulating layer;

(d) forming an upper opening through an upper region of the resist laminate, the upper opening having a laterally broadening space in a middle portion of the resist laminate;

(e) forming a lower opening through a lower region of the resist laminate, the lower opening communicating the upper opening, having a limited size along a current direction, and having generally vertical side walls;

(f) etching the insulating layer exposed in the lower opening to form a gate electrode opening exposing the semiconductor substrate;

(g) performing a heat treatment of the resist laminate to ~~deform~~ move the side walls of the lower opening so that at least one of opposite ends of the lower region of the resist laminate at the lower opening is retarded from a corresponding end of the insulating layer and that the lower opening of the resist laminate has a forward taper shape upwardly and monotonically increasing a size of the lower opening along the current direction; and

(h) filling a gate electrode stem in the gate electrode opening and the lower opening and forming a head in the upper opening, the head having an expanded size along the current direction.

Claim 2 (Original): The method of manufacturing a semiconductor device according to claim 1, wherein the heat treatment in said step (g) is performed at a temperature lower than a glass transition temperature of the lower region of the resist laminate.

Claim 3 (Previously presented): The method of manufacturing a semiconductor device according to claim 1, wherein the heat treatment in said step (g) makes the opposite side walls of the lower opening facing in the current direction have a generally symmetric taper shape and be retarded from opposite ends of the insulating layer.

Claim 4 (Cancelled)

Claim 5 (Currently amended) A method of manufacturing a semiconductor device, comprising the steps in the following order [[of]]:

(a) preparing a semiconductor substrate having a plurality of element regions;

(b) forming a resist laminate on the semiconductor substrate;

(c) applying an energy beam to an upper region of said resist laminate for defining an upper opening in each of said plurality of element regions, and applying an energy beam to a

lower region of said resist laminate in at least part of said plurality of element regions at a different dose depending on the element region;

(d) forming the upper opening through the upper region of the resist laminate in each of the plurality of element regions, the upper opening having a laterally broadened middle space;

(e) forming a lower opening through the lower region of the resist laminate in each of the element regions, the lower opening communicating the upper opening, having a limited size along a first direction, and having generally vertical side walls;

(f) performing a heat treatment of the resist laminate to deform the side walls of the lower opening in at least some of the element regions in accordance with doses so that the lower opening has a taper shape upwardly and monotonically increasing a size of the lower opening along the first direction; and

(g) filling a conductive stem in the lower opening and forming a head in the upper opening, the head having an expanded size along the first direction.

Claim 6 (Currently amended): A method of manufacturing a semiconductor device, comprising the steps in the following order [[of]]:

(a) preparing a semiconductor substrate having a plurality of element regions;

(b) forming a resist laminate on the semiconductor substrate;

(c) forming an upper opening through an upper region of the resist laminate in each of the plurality of element regions, the upper opening having a laterally broadening middle space;

(d) applying an energy beam to a lower region of the resist laminate in at least some of the element regions at a different dose corresponding to each element region;

(e) forming a lower opening through the lower region of the resist laminate in each of the element regions, the lower opening communicating the upper opening, having a limited size along a first direction, and having generally vertical side walls;

(f) performing a heat treatment of the resist laminate to deform the side walls of the lower opening in at least some of the element regions in accordance with doses so that the lower opening has a taper shape upwardly and monotonically increasing a size of the lower opening along the first direction; and

(g) filling a conductive stem in the lower opening and forming a head in the upper opening, the head having an expanded size along the first direction.

Claims 7-11 (Cancelled)

Claim 12 (Previously presented): A method of manufacturing a semiconductor device according to claim 1,

wherein said semiconductor substrate has a plurality of element regions, each having current input/output regions, said step (d) forms an upper opening in each of the element regions, said steps (e) to (h) are performed on each of the element regions, further comprising the step of:

(i) between the steps (d) and (e), applying an energy beam to a lower region of the resist laminate at different dose depending on the element region.

Claim 13 (Previously presented): A method of manufacturing a semiconductor device according to claim 12, wherein said step (g) forms the side walls of the lower opening having different taper angles.

Claim 14 (New) The method of manufacturing a semiconductor device according to claim 1, wherein said step (d) includes the sub-step of:

(d-1) applying a first electron beam to an upper region of the resist laminate, registered with said upper opening.

Claim 15 (New) The method of manufacturing a semiconductor device according to claim 14, wherein said step (d) further includes the sub-steps of:

(d-2) developing an upper portion of the resist laminate in the region applied with said first electron beam to form an upper window; and

(d-3) etching a middle portion of the resist laminate through said upper window to form said laterally broadening space.

Claim16 (New) The method of manufacturing a semiconductor device according to claim 15, wherein said step (e) includes the sub-steps of:

(e-1) applying a second electron beam to a lower region of the resist laminate, registered with said lower opening, through said upper window and said laterally broadening space; and

(e-2) developing an lower portion of the resist laminate in the region applied with said electron beam to form said lower opening.

Claim 17 (New) The method of manufacturing a semiconductor device according to claim 16, wherein said step (c) contains the sub-steps of:

(c-1) coating a lower electron beam resist layer on the insulating layer;

(c-2) baking the lower electron beam resist layer below a glass transition temperature of the lower electron beam resist layer; and

(c-3) coating a soluble resist layer on the lower electron beam resist layer, and coating an upper electron beam resist layer on the soluble resist layer.

Claim 18 (New) The method of manufacturing a semiconductor device according to claim 17, wherein the heat treatment in said step (g) is performed at a temperature below a glass transition temperature of the lower electron beam resist layer.

Claim 19 (New) The method of manufacturing a semiconductor device according to claim 18, wherein said forward taper shape has a general symmetric taper angle.

Claim 20 (New) The method of manufacturing a semiconductor device according to claim 5, wherein said energy beam applied to the upper region and the lower region in said step (c) is electron beam.

Claim 21 (New) The method of manufacturing a semiconductor device according to claim 20, wherein said step (e) includes the sub-steps of:

(e-1) applying an electron beam to a lower region of the resist laminate, registered with said lower opening, through said upper opening; and

(e-2) developing a lower portion of the resist laminate in the region applied with said electron beam in said step (e-1) to form said lower opening.

Claim 22 (New) The method of manufacturing a semiconductor device according to claim 6, wherein said energy beam in said step (d) is electron beam.